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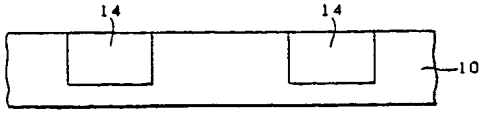
(54) Method of fabricating isolation trenches in a semiconductor wafer.

(57) A method for forming dielectric filled isolation trenches in a semiconductor, substrate wherein the substrate is coated with a photopolymer layer 14 which also fills the trenches. Depending on the type of radiation used, the photopolymer layer 14 is masked except for the regions directly above the filled trenches 12. The structure is exposed to radiation through the mask, which mask is then removed. The unexposed portions of the photopolymer layer 14 are washed away and heat is gradually applied to shrink the remaining photopolymer into the trenches 12 until it becomes coplanar with the semiconductor substrate surface. A mask is used if the radiation is ultraviolet light, but no mask is required if electron beam or x-radiation is employed.

FIG.1

FIG.5



EP 0 199 965 A2

METHOD OF FABRICATING ISOLATION TRENCHES IN A SEMICONDUCTOR WAFER

The present invention relates to the formation of trenches in the surface of a semiconductor wafer which are filled with dielectric material for isolating regions of the semiconductor.

Examples of prior art techniques are found in the following references.

US Patent 4,385,975, issued May 31, 1983 to Chu et al entitled METHOD OF FORMING WIDE, DEEP :DIELECTRIC FILLED ISOLATION TRENCHES IN THE SURFACE OF A SILICON SEMICONDUCTOR SUBSTRATE describes a method of forming a wide deep dielectric filled isolation trench in the surface of a silicon semiconductor substrate by forming a wide plug of chemical vapour deposited silicon dioxide in the trench, filling the remaining unfilled trench portions by chemical vapour depositing a layer of silicon dioxide over the substrate and etching back this layer. The method produces chemically pure, planar wide deep dielectric filled isolation trenches and may also be used to simultaneously produce narrow deep dielectric filled isolation trenches.

US Patent 4,307,180 issued December 22, 1981 to Pogge entitled PROCESS OF FORMING RECESSED DIELECTRIC REGIONS IN A MONOCRYSTALLINE SILICON SUBSTRATE describes a method of forming surface planarity to a substrate during removal of excess dielectric material when fabricating recessed regions of dielectric material in a semiconductor device wherein a dielectric layer is formed on the surface of the silicon substrate, a relatively thick layer of polycrystalline silicon deposited over the SiO_2 layer, openings formed through the polycrystalline layer and SiO_2 layer and into the substrate to form trenches, vapour depositing a layer of dielectric material over the surface of the substrate to a depth sufficient to fill the trench, depositing a planarized layer over a layer of dielectric material, reactive ion etching the planarizing layer, the dielectric layer, the polycrystalline layer, and selectively removing the remaining polycrystalline silicon layer to expose the SiO_2 layer.

US Patent 4,016,017 issued April 5, 1977 to Aboaf et al entitled INTEGRATED CIRCUIT ISOLATION STRUCTURE AND METHOD FOR PRODUCING THE ISOLATION STRUCTURE describes a process for fabricating a semiconductor device having a pattern of oxidized and densified porous silicon regions extending onto one of its major surfaces for isolating regions of the semiconductor. The process involves forming porous silicon regions in the surface of the semiconductor body such as a silicon wafer, i the ares where dielectric isolation between semiconductor devices is desired. The porous silicon regions are then oxidized at a temperature sufficient to completely oxidize porous silicon extends above the surface of the semiconductor wafer. The oxidized porous silicon regions are then subjected to a temperature higher than the oxidizing temperature utilized in the previous step to cause the densification of the oxidized porous silicon regions. The result of this densification step is the collapse of the porous oxide to a dense structure which is substantially planar with the surface semiconductor wafer.

US Patent 4,104,086 issued August 1, 1978 to Bondur et al entitled METHOD FOR FORMING ISOLATED REGIONS OF SILICON UTILIZING REACTIVE ION ETCHING describes a method for isolating regions of silicon involving the formation of openings that have a suitable taper in a block of silicon, thermally oxidizing the surfaces of the openings, and filling the openings with a dielectric material to isolate regions of silicon within the silicon block. The method is particularly useful wherein the openings are made through a region of silicon having a layer of a high doping conductivity.

US Patent 4,404,736 issued September 20, 1983 to Koshino et al entitled METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE OF MESA TYPE describes a method for manufacturing a semiconductor device of mese type which comprises forming mesa recesses of predetermined depth around an element in the surface of a semiconductor body, forming on the back of semiconductor body a film for lessening the concentration of stress, filling glass powder into mesa recesses, and sintering glass powder to form glass insulators. According to the method of the present invention, cracks can be prevented from being causes in the semiconductor body and glass insulators formed in mesa recesses.

US Patent 4,404,735 issued September 20, 1983 to Sakurai entitled METHOD FOR MANUFACTURING A FIELD ISOLATION STRUCTURE FOR A SEMICONDUCTOR DEVICE describes a method for forming a field isolation structure for semiconductor substrate, an insulating layer is formed on the substrate, an insulating layer is formed n the substrate at least in the groove, a glass layer or a silicon layer is formed thereon, and thereafter a high energy beam such as a laser beam is irradiated onto the glass or silicon layer to selectively heat the same thereby to melt or fluidify the layer and let the same flow into the groove is disclosed. A smooth and flat surface is obtained through the above melting process, which also prevents elec-

trical breaks in wiring layers formed thereon. The method is particularly suited to producing small field isolation structures thus improving the integration density of the device.

US Patent 4,420,874 issued December 20, 1983 to Funatsu entitled METHOD OF PRODUCING AN IIL SEMICONDUCTOR DEVICE UTILIZING SELF-ALIGNED THICKENED OXIDE PATTERNS describes a semiconductor device having an elementary region which is isolated by V-shape grooves from the other portions of the device, said semiconductor device comprising an insulating layer coating covering the surface of the semiconductor body of the device, wherein an injector region is formed under said insulating layer, and base regions are formed under said insulating layer between said thicker portions of said insulating layer and said V-shape grooves.

The prior art listed above is representative of the state of the art prior to the present invention and does not anticipate or make obvious the inventive features described hereinbelow.

An object of the present invention is to provide an improved method of forming isolation regions in a semiconductor wafer by dielectric-filled trenches.

Another object of the present invention is to provide an improved method of filling isolation trenches in a semiconductor wafer using photopolymer material, the excess portions of which are removed by washing.

A still further object of the present invention is to provide an improved method of filling isolation trenches in a semiconductor wafer using photopolymers which can be shrunk by ramped heat treatment.

Accordingly the invention provides a process for forming dielectric filled isolation trenches in the surface of a semiconductor substrate structure containing unfilled trenches comprising the steps of: coating said surface of said semiconductor substrate with photopolymer material such that said photopolymer material fills said trenches, exposing said masked semiconductor structure with radiation to photo expose said photopolymer coated regions above said trenches, washing away unexposed regions of said photopolymer coating, and applying heat to said semiconductor substrate structure to cause said exposed photopolymer material on said trenches to shrink until said photopolymer material in said trenches is coplanar with said surface of said semiconductor substrate.

The invention will now be more particularly described with reference to the accompanying drawings, in which:-

FIG. 1 through FIG. 5 are schematic illustrations of a cross section of a typical semiconductor wafer with trenches showing the steps in the process for filling the trenches with dielectric material.

Referring to FIG. 1, a schematic illustration of a semiconductor wafer 10 having trenches 12 formed therein in a manner well known in the prior art such as by a photolithographic masking technique.

FIG. 2 shows the semiconductor wafer 10 coated with a photopolymer 14 which fills the trenches as well as coats the surface of the wafer 10.

In FIG. 3, a mask 16 is provided which blocks the surface of the coated wafer except for the regions directly over the trenches 12. The mask 16 may preferably be the same mask used to delinear the trenches in the photolithographic process employed to produce the structure of FIG. 1. The mask 16 is only required when the exposing radiation is light. If the radiation is provided by an electron beam device or x-ray device, the electron or x-ray beam may be directed and confined onto the region above the photopolymer filled trench without the need for a mask.

The coated wafer structure 10 is then exposed to actinic radiation which may be ultraviolet light, electron beam radiation or x-rays. In the case of ultraviolet light, the light 18 is passed through the mask 16 as also illustrated in FIG. 3. The light 18 passes through mask 16 and exposes the portions of the photopolymer 14 above trenches 12.

The mask 16 is then removed and the photopolymer layer 14 is washed, causing the unexposed portions to be removed and leaving crosslinked photopolymer 14 in the trenches 12, and in the region above the trenches 12 (overfill) by the thickness of the original photopolymer coating 14 on the surface of the wafer. The resultant structure is shown in FIG. 4.

The wafer structure is next subjected to a ramped heat treatment which causes the remaining photopolymer 14 to shrink and recede into the trenches 12 until it is coplanar with the surface of wafer 10. This shrinking is possible because the photopolymer 14 has a composition which includes a solvent or compositional instability which makes such shrinkage practicable. Thus, the resultant structure illustrated in FIG. 5 is self-planarized.

The range of photopolymers which may be employed in the described process is large. The photofill does not depend on the particular type of polymer, however, there are several types which are preferred for their advantages. For example, polymide based resists are available and photopolymerizable siloxane-based compounds are available with high temperature and electrical properties similar to those of polymide which crosslink exposure to actinic radiation. Also, photopolymers and photocross-linkable compounds based on silicic acid are useful for avoiding high temperature restrictions. Since silicic acid compounds can be formed with 70% to 80% silicon dioxide, shrinkeage can be controlled as well as the avoidance of high temperature restrictions.

What has been described is a technique for filling isolation trenches in a semiconductor wafer with dielectric material which requires no back-etching and which can be shrunk back into the trenches by a controlled ramp heat application until the trench surface is coplanar with the wafer surface. Also, during fabrication, the unexposed or undesired dielectric material may be removed from the wafer surface by simply washing rather than etching.

Claims

1. A process for forming dielectric filled isolation trenches in the surface of a semiconductor substrate structure containing unfilled trenches comprising the steps of coating said surface of said semiconductor substrate with photopolymer material such that said photopolymer material fills said trenches, exposing said masked semiconductor structure with radiation to photo expose said photopolymer coated regions above said trenches, washing away unexposed regions of said photopolymer coating, and applying heat to said semiconductor substrate structure to cause said exposed photopolymer material on said trenches to shrink until said photopolymer material in said trenches is coplanar with said surface of said semiconductor substrate.

2. A method according to claim 1 wherein said photopolymer material is a polymide based photoresist.

3. A method according to claim 1 wherein said photopolymer material is a photopolymerizable siloxane-based compound.

4. A method according to claim 1 wherein said photopolymer material is a silicic compound containing 70% to 80% silicon dioxide.

5. A method according to claim 1 wherein said radiation in said exposing step is electron beam radiation.

6. A method according to claim 1 wherein said radiation used in said exposed step is x-radiation.

7. A method according to claim 1 further including, prior to said exposing step, the step of masking said coated semiconductor substrate surface with a light opaque mask having openings therein above said trench regions, and the step of removing said mask after said exposing step and washing away unexposed regions of said photopolymer coating, and wherein said radiation in said exposing step is ultraviolet radiation.

FIG.1

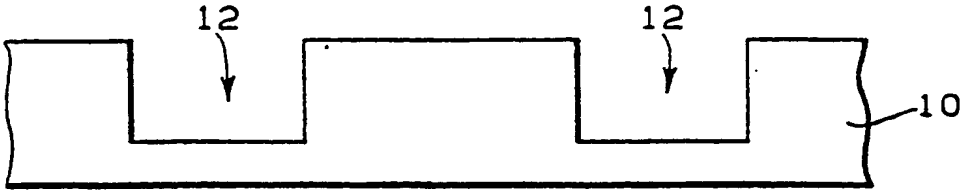


FIG.2

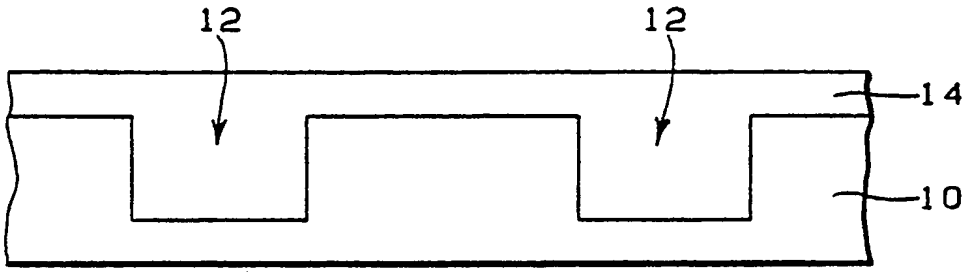


FIG.3

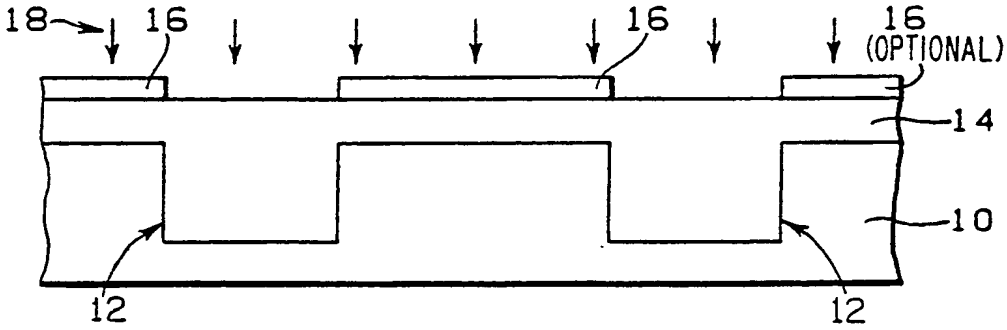


FIG.4

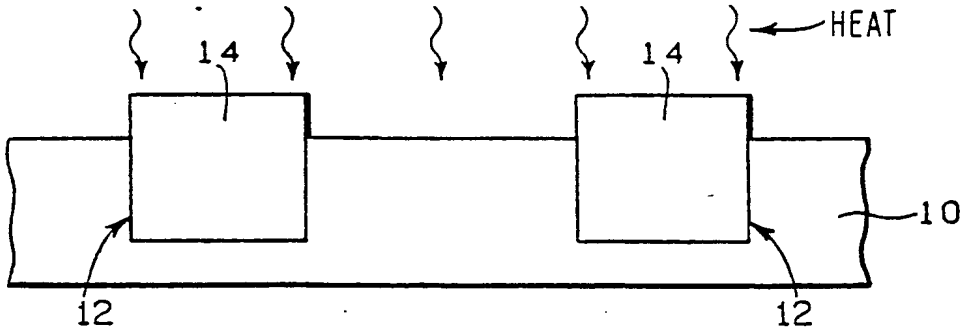
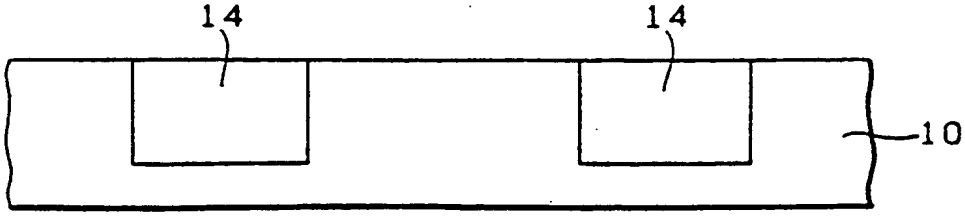


FIG.5



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EP 0 199 965 A3

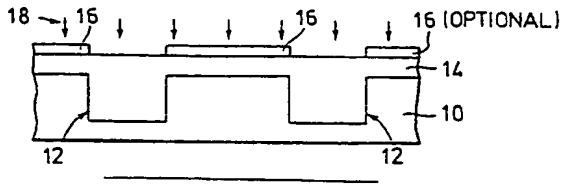

Fig 3.

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EUROPEAN SEARCH REPORT

Application Number

EP 86 10 3743

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 4A, September 1984, pages 1836-1837, New York, US; J. GRESCHNER et al: "Method of evenly filling isolation trenches" * Whole communication *	1,2,7	H 01 L 21/76 H 01 L 21/312
E	EP-A-0 178 500 (IBM) * Claims 1,2,6 *	1,2,5,7	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	13-07-1989	VANCRAEYNEST F.H.

CATEGORY OF CITED DOCUMENTS

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